

Digital Electronics II

Name _____ ID _____ TA _____

Partners _____

Date _____ Section _____

Please turn off the power of the Circuit Trainer when you connect the wires to the chips. Otherwise, the chips will be burned.

1. The test of DeMorgan's theorem

- The verification of $\overline{A \cdot B} = \overline{A} + \overline{B}$. (The TA will show how to do this part. So please copy what he/she did in the spaces provided.)

| $\overline{A \cdot B}$ | *Truth Table | | | | | | | | | | | | | | | | | | |
|------------------------|---|----------------------------|---|----------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| *circuit diagram | <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="width: 15%;">A</th> <th style="width: 15%;">B</th> <th style="width: 70%;">Y = $\overline{A \cdot B}$</th> </tr> </thead> <tbody> <tr><td> </td><td> </td><td> </td></tr> <tr><td> </td><td> </td><td> </td></tr> <tr><td> </td><td> </td><td> </td></tr> <tr><td> </td><td> </td><td> </td></tr> <tr><td> </td><td> </td><td> </td></tr> </tbody> </table> | A | B | Y = $\overline{A \cdot B}$ | | | | | | | | | | | | | | | |
| A | B | Y = $\overline{A \cdot B}$ | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | |

| $\overline{A + B}$ | *Truth Table | | | | | | | | | | | | | | | | | | |
|--------------------|---|------------------------|---|------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| *circuit diagram | <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="width: 15%;">A</th> <th style="width: 15%;">B</th> <th style="width: 70%;">Y = $\overline{A + B}$</th> </tr> </thead> <tbody> <tr><td> </td><td> </td><td> </td></tr> <tr><td> </td><td> </td><td> </td></tr> <tr><td> </td><td> </td><td> </td></tr> <tr><td> </td><td> </td><td> </td></tr> <tr><td> </td><td> </td><td> </td></tr> </tbody> </table> | A | B | Y = $\overline{A + B}$ | | | | | | | | | | | | | | | |
| A | B | Y = $\overline{A + B}$ | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | |

- The verification of $\overline{\overline{A} + \overline{B}} = \overline{\overline{A \cdot B}}$. (You will draw the circuit diagrams and truth tables. In addition, you are going to **see if the truth table is correct with the actual connections on the "Circuit Trainer."**)

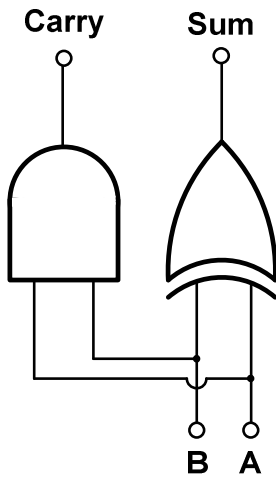
| $\overline{\overline{A} + \overline{B}}$ | *Truth Table | | | | | | | | | | | | | | | | | | |
|--|---|--|---|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| *circuit diagram | <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="width: 15%;">A</th> <th style="width: 15%;">B</th> <th style="width: 70%;">Y = $\overline{\overline{A} + \overline{B}}$</th> </tr> </thead> <tbody> <tr><td> </td><td> </td><td> </td></tr> <tr><td> </td><td> </td><td> </td></tr> <tr><td> </td><td> </td><td> </td></tr> <tr><td> </td><td> </td><td> </td></tr> <tr><td> </td><td> </td><td> </td></tr> </tbody> </table> | A | B | Y = $\overline{\overline{A} + \overline{B}}$ | | | | | | | | | | | | | | | |
| A | B | Y = $\overline{\overline{A} + \overline{B}}$ | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | |

$$\overline{A \cdot B}$$

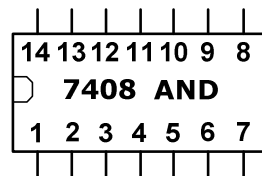
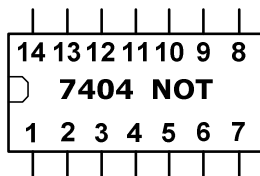
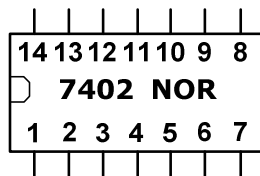
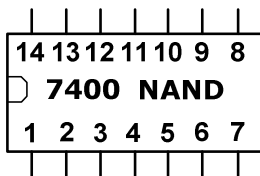
*Truth Table

| | | | |
|------------------|---|---|----------------------------|
| *circuit diagram | A | B | $Y = \overline{A \cdot B}$ |
| | | | |
| | | | |
| | | | |
| | | | |

2. Implementation of a half adder circuit



- Draw the wire connections for the half adder.



Please show (perform) your results to the TA before you leave. Thanks!

Lab Procedure for Digital Electronics II

Please turn off the power of the Circuit Trainer when you connect the wires to the chips. Otherwise, the chips will be burned.

1. The test of DeMorgan's theorem

- **Connect pin #7 to Ground with one wire, and pin #14 to 5V with another wire.** Otherwise, you will not get right results.
- **As the TA explained for $\overline{A \cdot B} = \overline{A + B}$, prove the equation, $\overline{A + B} = \overline{A} \cdot \overline{B}$.**

Procedure:

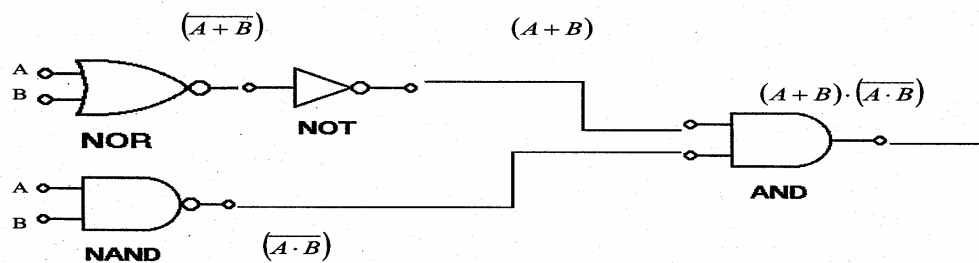
1. Draw the circuit diagram on the data sheet.
2. Guess the truth table by using the truth tables of the other gates.
3. If you like, you can draw the wire connections on a scratch paper. Then connect the wires on the breadboard to make sure if the equation is correct. (It must be correct!)

2. Implementation of a half adder circuit

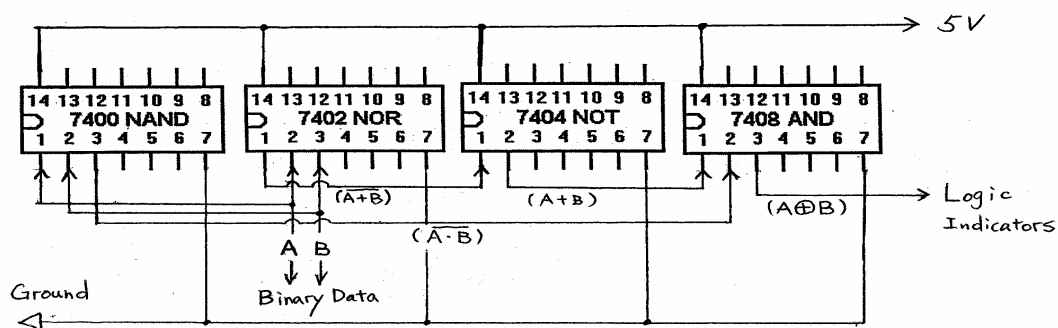
- **Make sure if pins #7 and pins #14 are connected to Ground and to 5V respectively.**
- **First, implement an XOR output.**

It is recommend you use this, $A \oplus B = (A + B) \cdot (\overline{A \cdot B})$ to implement XOR. Please refer to the following pictures.

◆ Circuit Diagram



◆ Actual Circuit Connections



- **Make sure if the XOR outputs are correct.**
Please see the reference paper that the TA provided for each table.
- **With referring to the circuit diagram on data sheet, implement the half adder circuit.**
Inputs, A and B will go to the LOGIC SWITCHES section on the Circuit Trainer so that you can change the combinations easily. (If those do not work, please use the Binary Data.)
According to the circuit, you must have 2 outputs. From the XOR gate, it will go to 'L0', and from the AND gate, it will go to L1 in the Logic Indicators so that it can be displayed easily.

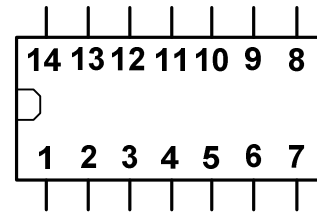
3. Lab report

- **Please state what you learned from this lab.**
This lab does not generate uncertainties or errors, so you will not discuss those. Of course, you can state what you did not understand on this lab.

References for Digital Electronics Labs

- **Pin connections of logic gates**

| pin # | 74LS00 NAND | 74LS02 NOR | 74LS04 NOT | 74LS08 AND |
|-------|----------------|---------------|---------------|---------------|
| 1 | 1A | 1Y | 1A | 1A |
| 2 | 1B | 1A | 1Y | 1B |
| 3 | 1Y | 1B | 2A | 1Y |
| 4 | 2A | 2Y | 2Y | 2A |
| 5 | 2B | 2A | 3A | 2B |
| 6 | 2Y | 2B | 3Y | 2Y |
| 7 | Ground | Ground | Ground | Ground |
| 8 | 3Y | 3A | 4Y | 3Y |
| 9 | 3A | 3B | 4A | 3A |
| 10 | 3B | 3Y | 5Y | 3B |
| 11 | 4Y | 4A | 5A | 4Y |
| 12 | 4A | 4B | 6Y | 4A |
| 13 | 4B | 4Y | 6A | 4B |
| 14 | Vcc | Vcc | Vcc | Vcc |

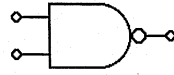


- **Truth tables**



AND

| A | B | Y_{AND} |
|---|---|-----------|
| 0 | 0 | 0 |
| 0 | 1 | 0 |
| 1 | 0 | 0 |
| 1 | 1 | 1 |



NAND

| A | B | Y_{NAND} |
|---|---|------------|
| 0 | 0 | 1 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 0 |



OR

| A | B | Y_{OR} |
|---|---|----------|
| 0 | 0 | 0 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 1 |



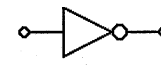
NOR

| A | B | Y_{NOR} |
|---|---|-----------|
| 0 | 0 | 1 |
| 0 | 1 | 0 |
| 1 | 0 | 0 |
| 1 | 1 | 0 |



XOR

| A | B | Y_{XOR} |
|---|---|-----------|
| 0 | 0 | 0 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 0 |



**NOT
(Inverter)**

| A | Y_{NOT} |
|---|-----------|
| 0 | 1 |
| 1 | 0 |